

WHAT IS CLAIMED IS:

1. A time shift circuit for a semiconductor test system for changing a delay timing of a portion of a test pattern for testing a semiconductor device, comprising:

5 a multiplexer for selectively producing delay value data indicating a value of time shift for a specific portion of test pattern in response to a shift command signal;

10 a vernier delay unit for producing timing vernier data based on programmed delay data prepared in the semiconductor test system and the delay value data selected by the multiplexer; and

15 a timing generator for generating a timing edge for the specific portion of the test pattern based on the timing vernier data from the vernier delay unit;

20 wherein the shift command signal sets either a normal mode where predetermined delay value data is selected by the multiplexer or a time shift mode where delay value data for shifting the timing edge in real time is selected by the multiplexer.

2. A time shift circuit as defined in Claim 1, wherein the vernier delay unit, comprising:

25 an adder for summing the programmed delay data and the selected delay value data from the multiplexer;

 a decoder for decoding higher bits of output data of the adder to produce a register select signal; and

30 a series of delay registers for delaying the timing vernier data configured by lower bits of the output data of the adder where one of the delay registers is selected by the register select signal to receive the timing vernier data as a first delay register.

3. A time shift circuit as defined in Claim 2, wherein the timing vernier data is shifted in the series of

delay registers starting from the first delay register at each clock, thereby producing the timing vernier data at a timing which is an integer multiple of a clock period.

4. A time shift circuit as defined in Claim 1,
5 wherein the timing generator includes a fine delay circuit for receiving the timing vernier from the vernier delay unit and producing a delay time which is smaller than one cycle of the clock based on the timing vernier data.

5. A time shift circuit for a semiconductor test
10 system for changing a delay timing of a portion of a test pattern for testing a semiconductor device, comprising:

a counter for transferring delay value data in a normal mode and incrementing the delay value data in an AC parametric measurement mode to determine a delay
15 timing of a portion of the test pattern applied to a device under test where a mode selection signal selects either the normal mode or the AC parametric measurement mode;

a vernier delay unit for producing timing vernier
20 data based on programmed delay data prepared in the semiconductor test system and the delay value data received from the counter;

a timing generator for generating a timing edge
25 for the specific portion of the test pattern based on the timing vernier data from the vernier delay unit;

means for stroking an output signal of the device under test at the timing edge from the timing generator; and

a strobe recovery circuit for determining pass or
30 fail status of the output signal of the device under test and producing a fail signal when the output signal fails;

wherein the fail signal is provided to the counter during the AC parametric measurement mode to increment

the delay value data, thereby continuously shifting the timing edge for stroking the output signal of the device under test until a change of state in the output signal is detected.

5 6. A time shift circuit as defined in Claim 5, wherein the vernier delay unit, comprising:

an adder for summing the programmed delay data and the selected delay value data from the multiplexer;

10 a decoder for decoding higher bits of output data of the adder to produce a register select signal; and

15 a series of delay registers for delaying the timing vernier data configured by lower bits of the output data of the adder where one of the delay registers is selected by the register select signal to receive the timing vernier data as a first delay register.

20 7. A time shift circuit as defined in Claim 6, wherein the timing vernier data is shifted in the series of delay registers starting from the first delay register at each clock, thereby producing the timing vernier data at a timing which is an integer multiple of a clock period.

25 8. A time shift circuit as defined in Claim 5, wherein the timing generator includes a fine delay circuit for receiving the timing vernier from the vernier delay unit and producing a delay time which is smaller than one cycle of the clock based on the timing vernier data.